1530-1550, Break

1550-1710, Session 8A, NVM
8 (R), Breeze: User-Level Access to Non-Volatile Main Memory for Legacy Software
16 (R), R-Cache: A Highly Set-Associative In-Package Cache using Memristive Arrays
96 (R), A Highly Non-Volatile Memory Scalable and Efficient File System
197 (R), NVCool: When Non-Volatile Caches Meet Cold Boot Attacks

1550-1710, Session 8B, Test & Verification
117 (R), Guiding RTL Test Generation Using Relevant Potential Invariants
224 (R), Back-End Layout Reflection for Test Chip..
247 (R), How multi-threshold designs can protect analog IPs?
42 (S), Optimization of Mutant Space for RTL Test Generation
196 (S), A reliability study on CNNs for critical embedded systems

1830-2030, Conference Dinner

Wednesday, Oct 10, 2018

0800-0830, Breakfast

0900-1020, Session 9A, NoC & Synchronization
115 (R), DEC-NoC: An Approx. Framework based on Dynamic Error Control with Applications to Energy-efficient NoCs
207 (R), RETUNES: Reliable and Energy-Efficient NoC Arch.
325 (R), Accelerating Synchronization in Graph Analytics using Moving Compute to Data Model on Tilera TILE-Gx72
62 (S), Eca-Router : On Achieving Endpoint Congestion Aware Switch Allocation in the On-Chip Network

0900-1020, Session 9B, Potpouri 2
13 (R), Design and Evaluation of a PVT Variation-Resistant TRNG Circuit
348 (R), Hardware-based Probabilistic Threat Detection and Estimation for Embedded Systems
355 (R), Reverse Engineering of Split Manufactured Sequential Circuits using Satisfiability Checking
334 (R), Minimizing Thermal Variation in Heterogeneous HPC Systems with FPGA Nodes
219 (S), Accurate Performance Bounds Calculation for Dynamic Voltage-Frequency Islands in Best Effort Networks-on-Chip

1020-1040, Break

1040-1200, Session 10A, File System & Cloud
362 (R), A Compact AES Hardware Implementation Secure Against 1st-Order Side-Channel Attacks
104 (R), PFCG: Improving the Restore Performance of Package Datasets in Deduplication Systems
54 (S), OME: An Optimized Modeling Engine for Disk Failure Prediction in Hetero Datacenter
89 (S), Enabling Accurate Performance Isolation on Hybrid Storage Devices in Cloud Environment
139 (S), LEA: A Lazy Eviction Algorithm for SSD Cache in Cloud Block Storage
14 (S), Optimizing Virtual Resource Management for Consolidated NUMA Systems

1040-1200, Session 10B, FPGA & ML
165 (R), Fine-Grained Parallel Routing for FPGAs with Selective Expansion
188 (R), DEEP: Dedicated Energy-Efficient Approximation for Dynamically Reconfigurable Architectures
338 (R), Load Balance-Aware Multi-Core Parallel Routing for Large-Scale FPGAs
252 (R), Using Machine Learning to Predict Path-Based Slack from Graph-Based Timing Analysis

1200-1215, Closing

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ICCD 2018 Program

Sunday, Oct 7, 2018

1400-1800, Tutorial Sessions 1, 2
1600-1620, Coffee Break
1800-2000, Reception

Monday, Oct 8, 2018

0730-0800, Breakfast
0800-0830, Opening by GC & PC

0830-0930, Keynote 1, Fred Chong,
Closing the Gap between Quantum Algorithms and Machines with Hardware-Software Co-Design

0930-1050, Session 1, Best Papers Session
269 (R), Composable Template Attacks using Templates for Individual Architectural Components
105 (R), Thermal-aware 3D Symmetrical Buffered Clock Tree Synthesis
344 (R), Low-overhead microarchitectural patching for multicore memory subsystems
157 (R), Power Grab in Aggressively Provisioned Data Centers: What is the Risk and What Can Be Done About It

1050-1110, Break

1110-1230, Session 2A, SSD
6 (R), Pensieve: a Machine Learning Assisted SSD Layer for Extending the Lifetime
21 (R), Selective Compression Scheme for Read Performance Improvement on Flash Devices
99 (R), OSPADA: One-Shot Programming Aware Data Allocation Policy to Improve 3D NAND Flash Read Performance

1110-1230, Session 2B, Side Channels
186 (R), A Timing Side-Channel Attack on a Mobile GPU
251 (R), Analysis of Row Hammer Attack on STTRAM
285 (R), Machine Learning on the Thermal Side-Channel: Analysis of Accelerator-rich Architectures

1110-1230, Session 2A, SSD (continued)
138 (R), Cap: Exploiting Data Correlations to Improve the Performance and Endurance of SSD RAID

1230-1400, Lunch and Special Panel 1: Non-Volatile Memory: Will it be Memory, Storage, or Neither?

1410-1530, Session 3A, Security & Capability
108 (R), CheriRTOS: A Capability Model for Embedded Devices
198 (R), ReadPRO: Read Prioritization Scheduling in ORAM for Efficient Obfuscation in Main Memories
209 (R), SGXlinger: A New Side-channel Attack Vector Based on Interrupt Latency against Enclave Execution
324 (R), Breaking the Oblivious-RAM Bandwidth Wall

1410-1530, Session 3B, Microarchitecture
7 (R), Rearranging Random Issue Queue with High IPC and Short Delay
65 (R), Array Tracking Prefetcher for Indirect Accesses
158 (S), Dynamically Disabling Way-prediction to Reduce Instruction Replay
233 (S), Characterization of Ultra Low Power Branch Predictors ..
35 (S), OldSpot: A Pre-RTL Model for Fine-grained Aging and Lifetime Optimization
210 (S), SPF: Selective Pipeline Flush

1530-1550, Break

1550-1730, Session 4A, Logic & Circuit Design 1
68 (R), Power-Efficient ReRAM-Aware CNN Model Generation
111 (R), R-Accelerator: A Reconfigurable Accelerator with RRAM Based Logic Contraction and Resource Optimization …

1550-1730, Session 4B, Design Automation
191 (R), Software and Hardware Techniques for Reducing the Impact of Quantization Errors in Memristor Crossbar Arrays
203 (R), Trading Off Temperature Guardbands via Adaptive Approximations

1550-1730, Session 4A, (continued)
118 (R), 3D Crosspoint Memory as a Parallel Architecture for Computing Network Reachability
257 (R), Dynamic Computin in Memory (DCIM) in Resistive Crossbar Arrays
283 (R), Low Area-Delay Complexity Digit-Level Parallel-In Serial-Out Multiplier over GF(2^{m}) ..

1550-1730, Session 4B, (continued)
323 (R), Lattice-Traversing Design Space Exploration for High Level Synthesis

Tuesday, Oct 9, 2018

0750-0820, Breakfast

0820-0920, Keynote 2, Lin Zhong
Fixing the broken synergy at the hardware/software boundary

0930-1050, Session 5A, Novel Architectures
117 (R), Heuristic Approximation of Early-Stage CNN Data Representation for Vision Intelligence Systems
184 (R), Puppet: Energy Efficient Task Mapping For Storage-less and Converter-less Solar-Powered Non-volatile Sensor Nodes
275 (R), SyncVibe: Fast and Secure Device Pairing through Physical Vibration on Smartphones
351 (S), FPGA Virtualization in Cloud-based Infrastructures over Virtio
77 (S), Forca: Fast and Atomic Remote Direct Access to Persistent Memory

0930-1050, Session 5B, Memory 1
141 (R), CART: Cache Access Reorder. Tree for Efficient Cache & Mem. Accesses in GPUs
36 (R), ArchSampler: Architecture-Aware Memory Sampling Library for In-Memory Applications
234 (R), PIM-TGAN: A Processing-in-Memory Accelerator for Ternary Generative Adversarial Networks
86 (S), Path Prefetching: Accelerating Index Searches for In-Memory Databases
263 (S), Reducing Inter-Application Interferences in Integrated CPU-GPU Heterogeneous Architecture

1050-1110, Break

1110-1230, Session 6A, Memory 2
2 (R), Solar-DRAM: Reducing DRAM Access Latency by Exploiting the Variation in Local Bitlines
10 (R), Scalable and Efficient Virtual Memory Sharing in Heterogeneous SoCs with TLB Prefetching and MMU-Aware DMA Engine
48 (R), DR DRAM: Accelerating Memory-Read-Intensive Applications
19 (R), Puzzle Memory: Multifractional Partitioned Heterogeneous Memory Scheme

1110-1230, Session 6B, Logic & Circuit Design 2
15 (R), Synchronization of Ring-based Resonant Standing Wave Oscillators for 3D Clocking Applications
28 (R), Generalized Tree Architecture for Efficient Successive-Cancellation Polar Decoding
182 (R), Parameterized Posit Arithmetic Hardware Generator
120 (S), BGIM: Bit-Grained Instant-on Memory Cell for Sleep Power Critical Appslications
202 (S), Autonomous Temperature Management through Selective Control of Exact-Approx. Tiles

1230-1400, Lunch and Special Panel 2: Microarchitecture Side Channels: Implications for Computer Design

1410-1530, Session 7A, Accelerators & GPUs
97 (R), Automatic Mapping of the Sum-Product Network Inference Problem to FPGA-based Accelerators
142 (R), BLPP: Improving the Performance of GPGPUs …
175 (R), General IDS Acceleration for High-Speed Networks
239 (R), Scalable Multi-Queue Data Transfer Scheme for FPGA-based Multi-Accelerators

1410-1530, Session 7B, Potpouri 1
346(R), Characterizing 3D Charge Trap NAND Flash: Observations …
248 (R), A Plain-text Increment Compression (PIC) Technique …
1 (R), Towards Efficient Micoarchitecture Design of Simultaneous Localization and Mapping in Augmented Reality …
163 (S), Training Neural Networks with Low Precision Dynamic Fixed-Point
95 (S), Decentralized Collaborative Power Management through Multi-Device Knowledge Sharing