The IEEE International Conference on Computer Design encompasses a wide range of topics in the research, design and implementation of computer systems and their components. ICCD's multi-disciplinary emphasis provides an ideal environment for developers and researchers to discuss practical and theoretical work covering systems and applications, computer architecture, verification and test, design tools and methodologies, circuit design, and technology. We especially encourage original work submissions that look forward to future systems and technologies. Papers can be submitted in one of the following **five conference tracks:**

Computer Systems: Systems architecture (memory hierarchy, memory, storage, NoC), and systems software (compiler, programming language/model, OS, hypervisor, runtime) design and co-design for: embedded/real-time systems, IoT devices, high-performance computing servers, data center and cloud/edge servers; General purpose multi/many cores, co-processors, accelerators, and application-specific systems; Support for security, reliability, and energy efficiency and proportionality; Architecture and compiler for thread parallelism, synchronization, and communication; Virtual memory; System integration of emerging technologies: NVMs, quantum, etc.

Processor Architecture: Microarchitecture design techniques for single- and multi-core processors: instruction-level parallelism, pipelining, caching, branch prediction, multithreading; Techniques for low-power, secure, and reliable processors; Embedded, network, graphic, system-on-chip, application-specific and digital signal processor design; Hardware support for processor virtualization; Real-life design challenges: case studies, tradeoffs, postmortems.

Logic and Circuit Design: Circuits and design techniques for digital, memory, analog and mixed-signal systems; Circuits and design techniques for high performance and low power; Circuits and design techniques for robustness under process variability and radiation; Design techniques for emerging process technologies (MEMs, spintronics nano, quantum, flexible electronics); Asynchronous circuits; Signal processing, graphic processor and arithmetic circuits.

Electronic Design Automation: High-level, logic and physical synthesis; Physical planning, design and early estimation for large circuits; Automatic analysis and optimization of timing, power and noise; Tools for multiple-clock domains, asynchronous and mixed timing methodologies; CAD support for FPGAs, ASSPs, structured ASICs, platform-based design and NOC; DfM and OPC methodologies; System-level design and synthesis; Tools and design methods for emerging technologies (MEMs, spintronics, nano, quantum).

Test, Verification and Security: Design error debug and diagnosis; Fault modeling; Fault simulation and ATPG; Analog/RF Testing; Statistical Test Methods; Large volume yield Analysis and Learning; Fault tolerance; DFT and BIST; Functional, transaction-level, RTL, and gate-level modeling and verification of hardware designs; Equivalence checking, property checking, and theorem proving; Constrained-random test generation; High-level design and SoC validation. Hardware security primitives; Side channel analysis; Logic and microarchitectural countermeasures; Hardware security for IoT; Interaction between VLSI test and trust.

The full version of the paper should be a PDF file following the submission guidelines that is made available at the conference website. **See the ICCD 2018 website at http://www.iccd-conf.com for additional information.**

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